Mechanically Flexible Interconnects with Highly Scalable Pitch and Large Stand-off Height for Silicon Interposer Tile and Bridge Interconnection

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Abstract

This paper reports novel interconnect technologies to enable a large scale 'interposer tile' and 'silicon bridge' interconnection platform. Microfabricated self-alignment structures enable high alignment accuracy between the components. Mechanically flexible interconnects (MFIs) are utilized to enable rematable electrical interconnects. Moreover, a proof of concept demonstration with interposer tiles directly mounted on FR4 board and interconnected by silicon bridges is reported.

I. Introduction

Silicon interposer based 2.5D integration has received significant interest because it can provide a high-bandwidth and low-energy interconnect platform for heterogeneous systems [1-6]. However, for state-of-the-art 2.5D integrated systems, as shown in Figure 1 (a), the high performance interposer interconnections are only available for chips mounted on a single interposer. Given that the size of interposers is limited by the reticle size as well as cost, there exists a limit on the number of chips that can be integrated. Therefore, an innovative interconnection platform between interposers is needed to extend interconnect benefits over a large-scale system.

As shown in Figure 1 (b), we propose a novel vision to realize large scale multi-interposer systems using positive self-alignment structures (PSAS) and mechanically flexible interconnects (MFIs). 'Interposer tiles', which are essentially silicon interposers with alignment structures, can possibly be directly mounted on the motherboard (or package for some applications). The adjacent interposer tiles are interconnected by 'silicon bridges', which are silicon chips with MFIs and corresponding routing designs. The tile-to-motherboard and bridge-to-tile electrical interconnects are enabled by MFIs with various pitches and heights. Interposer tiles, silicon bridges and the motherboard (or package) are self-aligned with each other using PSAS and inverted pyramid pit pairs. Our proposed concept is an extension of the macro-chip concept demonstrated in [4-6]. Key features of our large scale silicon platform include the following:

1) Low-cost and high-accuracy self-aligned assembly of the components (i.e. motherboard, interposer tiles and silicon bridges) is obtained using PSAS and pyramid pit pairs [7]. Besides electrical interconnects shown in Figure 1 (b), the proposed interposer tile-silicon bridge platform can utilize silicon nanophotonic interconnects as well. Using a similar self-alignment capability, a 15Gpbs silicon photonic link with 300 fJ/bit has been demonstrated [4].

2) Fine pitch MFIs are used to enable high density and robust I/Os between interposer tiles and silicon bridges.

3) Highly flexible interconnects are used to mitigate the stress induced by the coefficient of thermal expansion (CTE) mismatch between the silicon interposer tile and the substrate, which could be an organic or ceramic package. Moreover, the silicon interposer tile may be directly mounted on the motherboard, which not only shortens the interconnect length, increases interconnect density, and minimizes impedance discontinuities, but also lowers the system package thickness.

4) The system level electrical interconnects (i.e. tile-to-bridge and tile-to-board) enabled by Au-NiW MFIs [9] and PSAS are rematable, therefore a system-level test can be accomplished before the permanent integration of all silicon interposer tiles and bridges. In state-of-the art 2.5D systems, as the number and diversity of chips increases, the system yield and cost suffer. However, in our proposed system, non-functional chips detected during testing can be replaced, which increases the system yield and lowers cost.

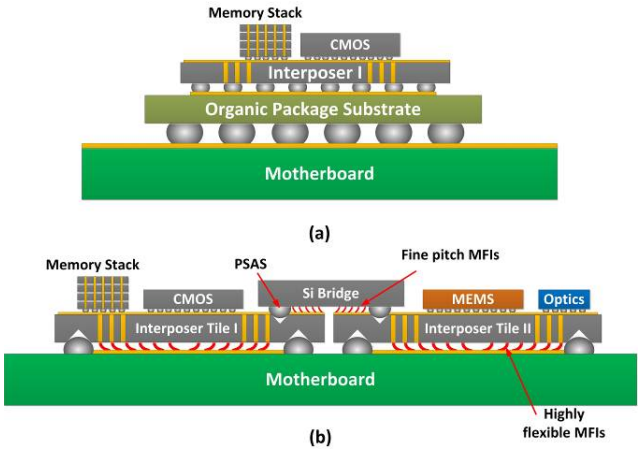


Figure 1: (a) State-of-the art 2.5D integration, (b) interposer tile and silicon bridge interconnection platform

PSAS and MFIs are the two key technologies to enable the envisioned system in Figure 1 (b). Since self-alignment assembly using PSAS was previously demonstrated in [7, 8], in this paper we focus on the MFIs, which are a key technology to enable our envisioned system shown in Figure 1 (b). Various flexible interconnect technologies have been investigated over the past decades [9-17]. However, it is very challenging for the traditional technologies to enable the above envisioned platform. In this paper, we report an MFI technology and process designed for silicon bridge-to-interposer tile and interposer tile-to-motherboard interconnections. Specifically, the reported MFI process can realize MFIs with a wide range of pitches (from 150 µm to 50 µm). Moreover, the reported MFIs feature a large vertical gap

and truncated-cone tip for improved temporary electrical interconnection. We also report PSAS fabrication on FR4 and the assembly of interposer tiles and bridges as a proof of concept demonstration of the envisioned large-scale platform in Figure 1 (b).

II. Advanced MFI Technology

In this section, a spray coating based fabrication process is demonstrated to enable MFI fabrication with a wide range of pitches, a large vertical gap and a truncated-cone tip. Four-point resistance measurements and mechanical indentation tests are also reported for the fabricated MFIs.

A. Spray Coating Based Fabrication

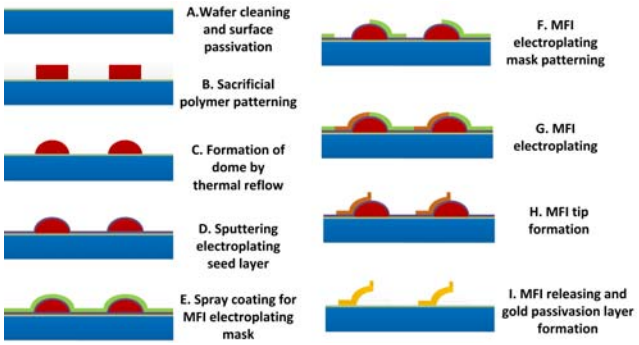


Figure 2: Spray coating based MFI fabrication process

The fabrication process of the MFIs is shown in Figure 2. The process begins with the formation of sacrificial polymer domes, which is accomplished by patterning and thermally reflowing a spin coated polymer layer on a nitride passivated silicon wafer [9,16,17]. Next, a Ti/Cu/Ti film is sputter coated on top of the 65 µm tall polymer domes as an electroplating seed layer. A thick conformal negative photoresist layer is next spray coated and patterned on top of the seed layer as the electroplating mold. Following the electroplating of MFIs, the photoresist plating mold is removed and followed by the patterning of another photoresist layer for the subsequent tip electroplating. Once the tips with a truncated-cone profile are formed on top of the MFIs, the tip electroplating mold, the seed layer and the polymer domes are stripped leaving behind MFIs with truncated-cone tips and a 65 µm vertical gap above the substrate. Finally, the free-standing NiW MFIs on the wafer are passivated by an electroless gold finish [9].

As shown in Figure 2, a key step to enable MFI fabrication is the spray coating of photoresist on the polymer domes. Because of the large height of the domes, a spin-coated photoresist process, similar to that used in prior flexible interconnects [10-15], would not work in this application.

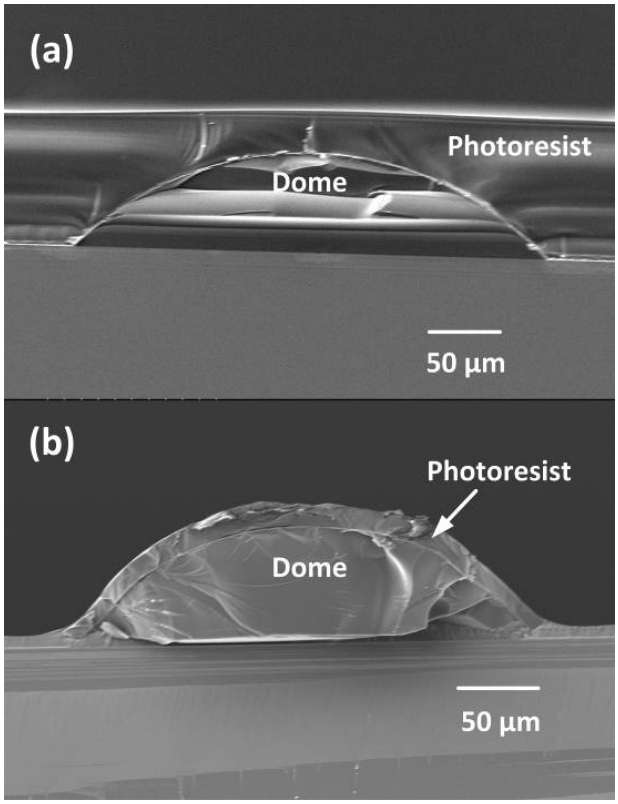


Figure 3: Compared to spin coating (a), photoresist spray coating (b) can form a uniform photoresist layer on top of sacrificial domes

Figure 3 (a) illustrates the photoresist layer coated over the substrate with domes by a traditional spin coating process. The photoresist layer is thin on top of the domes and thick in the valley between the domes. The non-uniform photoresist thickness makes the spin coating approach not feasible to fabricate the MFIs for the following reasons: 1) it is not possible to obtain a proper exposure and development simultaneously on top of the domes and in the valley between the domes; 2) a high soft bake temperature (> 110 °C) is needed for the thick photoresist in the valleys, but such high temperature softens the sacrificial polymer domes, which leads to breaking of the plated MFIs. The photoresist spray coating process solves these challenges. As shown in Figure 3 (b), a conformal photoresist layer can be formed over the surface of the domes by spray coating. Therefore, the exposure dose can be optimized since the thickness of the photoresist is identical both on the top of the domes and in the valleys. In addition, since the solvent evaporates quickly during the spray coating process, this precludes the need for a high temperature soft bake process. A possible drawback of spray coating is that surface roughness becomes worse as the thickness of photoresist layer increases. However, after a low temperature (<80 °C) oven bake step, the surface variation can be controlled to within 0.5 µm, as shown in Figure 4.

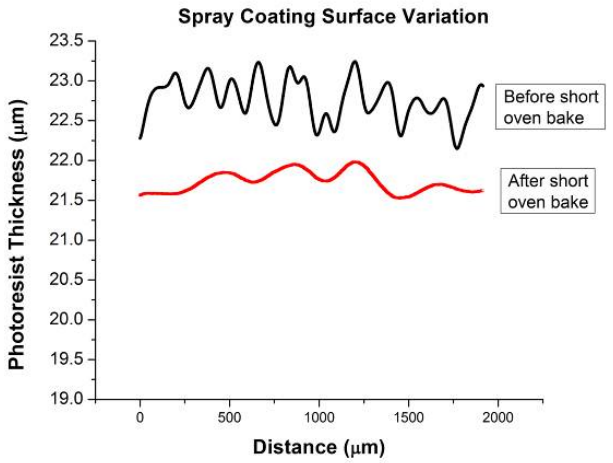


Figure 4: Surface roughness of the spray coated photoresist can be improved by a short oven bake step

B. MFIs with Highly Scalable Pitch

With the spray coating based process, wafer-level batch fabricated MFIs with highly scalable pitch can be attained. Such dense MFIs would be used for interposer tile-to-silicon bridge interconnection. Figure 5 illustrates 7.2 μm thick MFI array with a vertical gap of 65 μm and on 150μm, 75μm and 50 μm pitches.

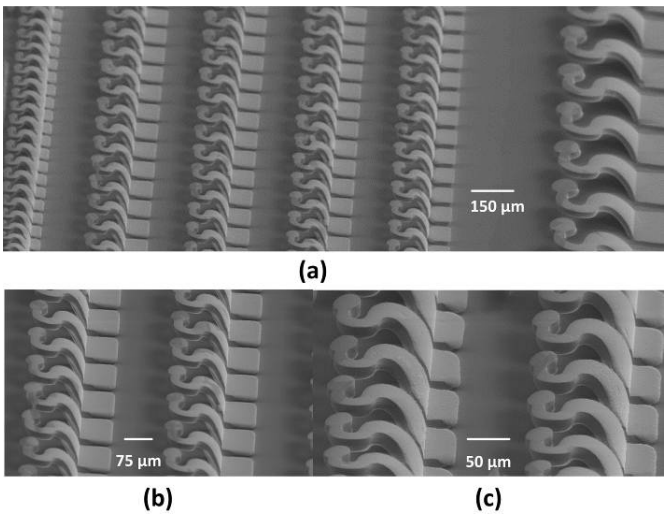


Figure 5: MFIs with highly scalable pitch (150 μm, 75 μm, and 50 μm), and a vertical gap of 65 μm

Four-point resistance measurement is performed using a probe station. During the measurements, the tested MFIs are partially bent to attain a stable resistance reading. The measured data is summarized in Table I and indicates that the resistance of the MFIs on different pitches does not vary appreciably. The MFIs with pitches of 150 μm to 50 μm are designed using the rules developed in [9,16,17] and scaled down in all dimensions except thickness with the same factor.

TABLE I
MEASURED RESISTANCE AND COMPLIANCE OF MFIS

Pitch (μm)	Average Resistance (mΩ)	Standard Deviation (mΩ)	Compliance (mm/N)
150	133.2	3.79	5.32
75	134.3	4.02	2.72
50	119.1	3.87	1.20

The mechanical deformation properties of MFIs are verified by indentation tests. Each indentation cycle includes a forward and a backward step. In the forward step, a predefined forced is applied on top of a free standing MFI by a piezo-driven indentation head, which bends the MFI to a specific depth. In the backward step, the MFI is released to recover its pre-indentation profile. The real-time position and reaction force of the tip are recorded in Figure 6 and the corresponding compliance of the MFIs is calculated and summarized in Table I. As shown in Figure 6, for a given thickness (7.2 μm), the compliance of MFIs decreases as the pitch scales. The compliance can be increased (to avoid rigid MFIs) by reducing the MFI thickness.

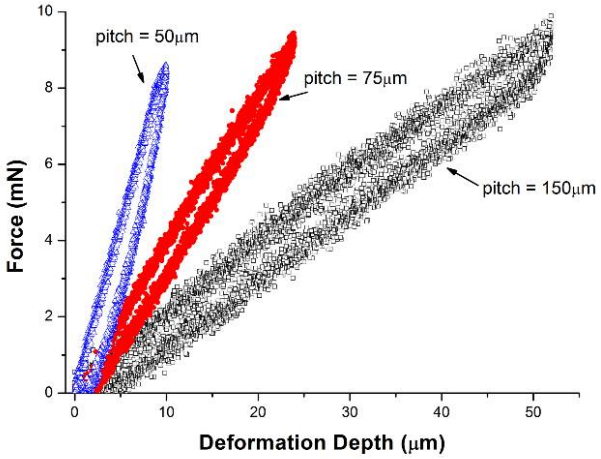
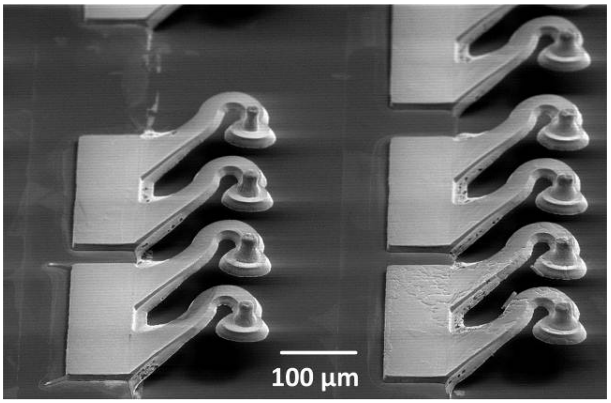


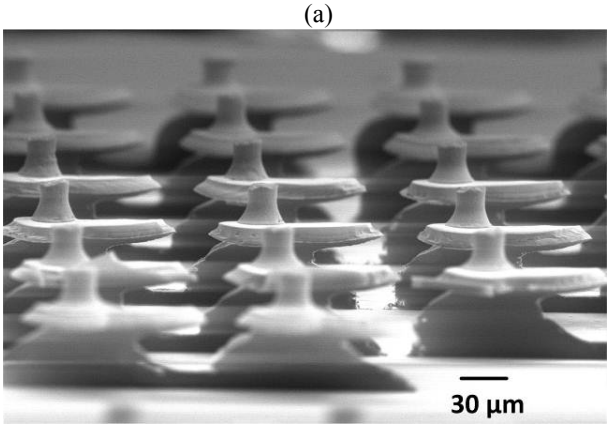
Figure 6: Indentation results of MFIs with pitches of 150 μm, 75 μm, and 50 μm

C. MFIs with truncated-cone tip

In order to overcome substrate surface variation and warpage, which is critical for interposer tiles on motherboard (or package) assembly, MFIs with truncated-cone tips are fabricated, as shown in Figure 7. The aggregate height of the MFI and tip is approximately 95 μm (65 μm tall vertical gap and 30 μm tall tip). The blunt tip can enhance the scratching capability while maintaining long tip life-time by avoiding tip plastic deformation, which occurs to sharp tips.



(a)



(b)

Figure 7: Overview (a) and front view (b) of Au-NiW MFIs with truncated-cone tip

Figure 8 illustrates gold-coated MFIs with truncated-cone tip. Compared with other passivation approaches, such as polymer coating, electroless gold passivation is a simple and low cost approach to enhance the life time of NiW MFIs as reported in [9]. In addition, the gold layer can lower the MFI resistance and MFI/pad contact resistance as well.

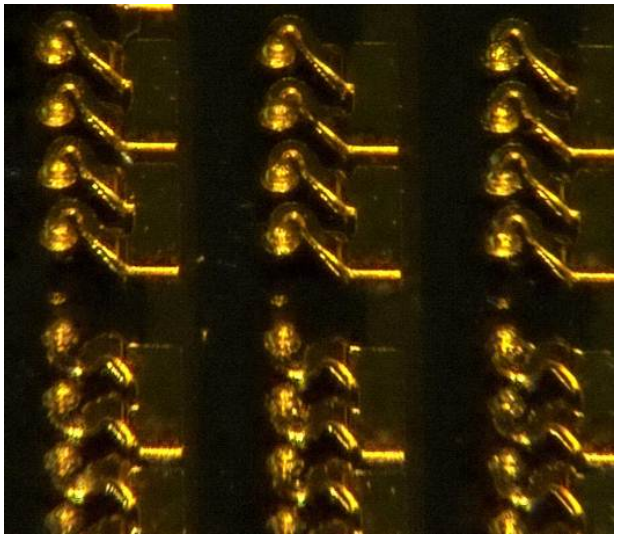


Figure 8: NiW MFIs after being passivated by electroless gold

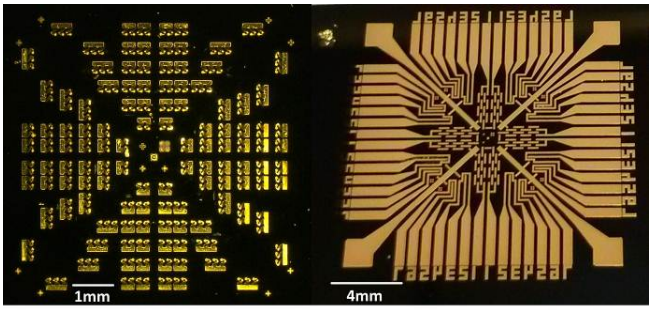
The experimental results of interposer tile assembly with MFIs are discussed next:

1) Test bed fabrication

To demonstrate the mechanical robustness of the MFIs, a special substrate was designed and fabricated: bonding pads with different heights were formed across the substrate. In this manner, the only way to attain electrical contact across the entire chip is for the MFIs to locally deform to mate with the variable height pads. In this test bed, the pad height variation was 45 µm. For comparison, a substrate with all uniform height pads was also fabricated. The test chip with MFIs is shown in Figure 9 (a). The substrate with uniform and non-uniform pad heights are shown in Figure 9 (b) and (c), respectively. A profilometer measurement of the pads with differing height is shown in Figure 10.

2) Assembly

The assembly demonstrations are performed using a Finetech flip-chip bonder to align and place the interposer tile with MFIs onto the substrate. After assembly, an X-ray imaging tool, Dage X-Ray XD7600NT, was used for assembly verification. As shown in Figure 11, the interposer tile with MFIs is well aligned with the test substrate.



(a) (b)

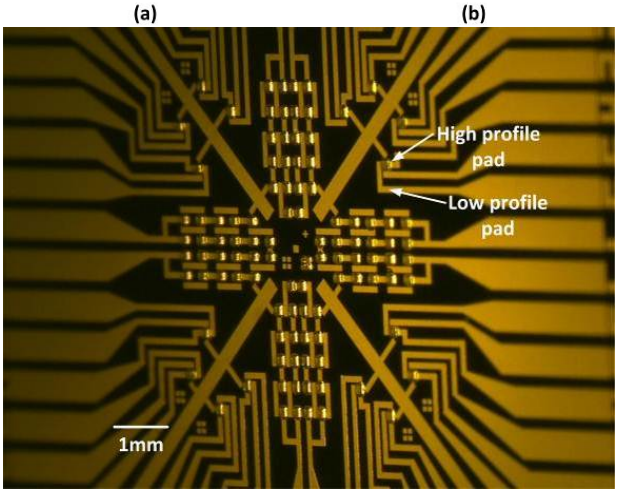


Figure 9: Interposer tiles with Au-NiW MFIs (a) and corresponding substrate with uniform pads (b) and non-uniform pads (c) for four-point resistance measurement.

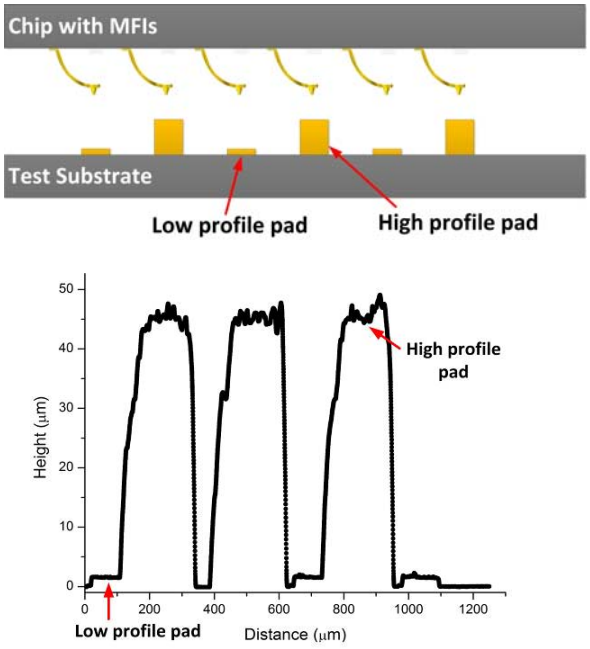


Figure 10: Assembly test bed cross-section and profilometer data of the non-uniform height pads on the substrate

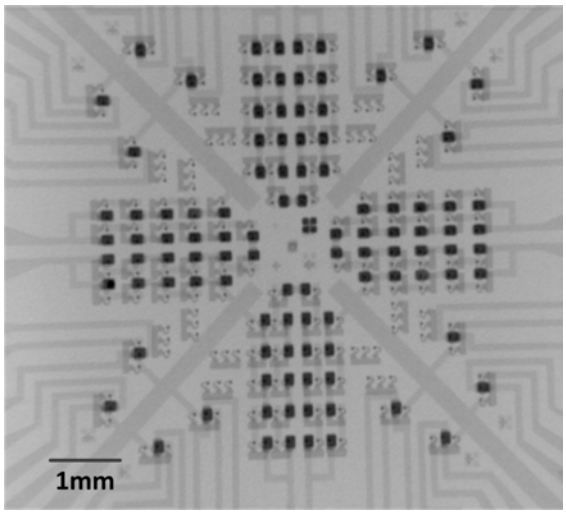
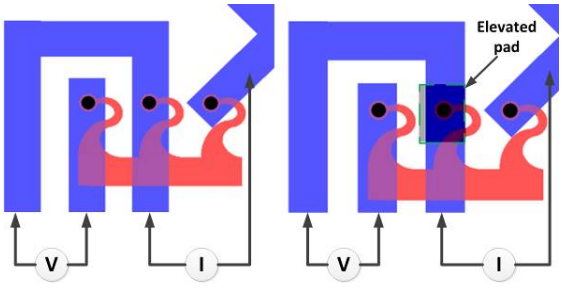


Figure 11: X-ray image of the assembled interposer tile and substrate with non-uniform pads



(a) (b)

Figure 12: Four-point measurement design for the assembled interposer tile with MFIs

The four-point test designs shown in Figure 12 were used to characterize the resistance of assembled MFIs. The measured results are plotted in Figure 13. The average resistance and the corresponding standard deviation are summarized in Table II. The results indicate that the resistance of MFIs assembled on the substrate with non-uniform height pads is slightly larger than those assembled on the substrate with uniform pads. The resistance difference is believed to be mainly from the larger contact resistance of MFIs assembled to elevated pads, which have worse contact interface than MFIs assembled to low-profile pads. As shown in Figure 10, the surface roughness of elevated pads (5 μm) is much larger than the low-profile pads (1μm).

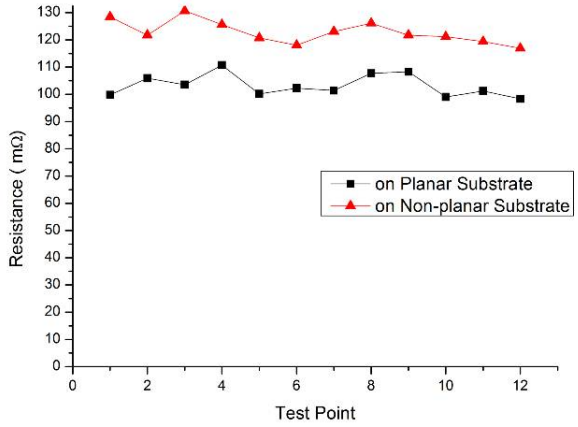


Figure 13: Four-point resistance measurements of MFIs assembled on substrates with uniform and non-uniform pads

TABLE II
RESISTANCE CHARACTERIZATION FOR REMATABLE ASSEMBLY

	Average Resistance (mΩ)	Standard Deviation (mΩ)
Assembly on substrate with uniform height pads	103.21	4.06
Assembly on substrate with non-uniform pads	122.81	4.16

III. Self-Aligned Interposer Tiles and Bridges Assembly on FR4

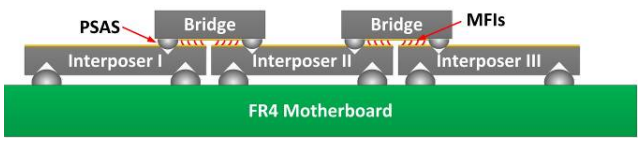


Figure 14: Self-aligned interposer tiles and bridges assembly on FR4 board using PSAS and MFIs

In this section, we report PSAS assisted assembly of interposer tiles and bridges on FR4 board, as shown in Figure 14. The demonstrated test bed contains: 1) three silicon

interposer tiles, which are essentially 20x20 mm^2 silicon interposers with inverted pyramid pits on both sides; 2) two 20x6 mm^2 silicon bridges with PSAS on the side facing the interposer tiles; 3) one large FR4 board with PSAS on the top side. The details of PSAS/pit pair and assembly process are discussed next.

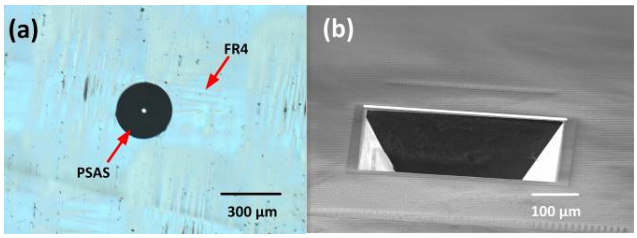


Figure 15: Key technologies enabling the proposed multi-interposer system: (a) PSAS, and (b) inverted pyramid pit

Figure 15 illustrates the key structures enabling the test bed: 1) the PSAS, as shown in Figure 15 (a), is a truncated polymer sphere with perfectly smooth surface and fabricated using a thermal reflow process; 2) the inverted pyramid pit structure, as shown in Figure 15 (b), is fabricated by an anisotropic silicon wet etch. The fabrication and characterization details of the PSAS and pits are reported in [7].

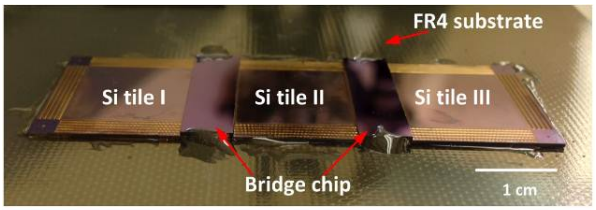


Figure 16: Self-aligned test bed includes three interposer tiles and two silicon bridge chips on FR4 board

As shown in Figure 16, three interposer tiles are mounted on top of the FR4 board. The position of each tile is determined by the PSAS on the FR4 board since they are designed to mate with the pits on the back side of the silicon tiles. Next, the silicon bridges are assembled across the adjacent tiles with PSAS side facing downward. Finally, all components of the test bed are glued by applying epoxy around the edge (this was used to simplify the mounting).

The alignment accuracy of the assembled test bed is measured by observing vernier patterns via infrared microscopy. As summarized in Table III and Table IV, the maximum misalignment between silicon interposer and FR4 is 4.4 µm; the maximum misalignment between silicon bridges and interposer tiles is at the top left corner of the bridge 2, which is about 7.6 µm. This alignment system, with further optimization, can be used to support silicon nanophotonic interconnection between silicon tiles using the silicon bridge.

TABLE III
PSAS ASSISTED SELF-ALIGNMENT ACCURACY OF SI/FR4

Regions	Si/FR4	
	Horizontal	Vertical
Bottom Left	4.4	2.0
Bottom Right	3.2	-3.2
Top Right	-1.6	-3.2
Top Left	-2.8	2.4

TABLE IV
PSAS ASSISTED SELF-ALIGNMENT ACCURACY OF BRIDGE/TILE

Regions	Si Bridge I		Si Bridge II	
	Horizontal	Vertical	Horizontal	Vertical
Bottom Left	-4.0	4.6	-5.2	-5.0
Bottom Right	-5.4	-4.8	-5.0	-5.0
Top Right	5.8	3.2	-5.8	-5.2
Top Left	6.0	-5.0	-7.6	-5.0

IV. Conclusion

Mechanically flexible interconnects featuring 1) a wide range of pitches (150 µm to 50 µm), 2) a vertical gap of 65 µm, and 3) a truncated-cone tip (30 µm tall) are reported in this paper. Assembly test beds to electrically and mechanically characterize the MFIs are also reported in this paper. Finally, an interposer tile and silicon bridge based system is demonstrated using PSAS assisted self-assembly.

Acknowledgments

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